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Attorney Docket No: NVID001/00US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of Priem et al.

Serial No.: 09/056,656 Examiner: Ulka J. Chauhan

Filed: April 7, 1998 Art Unit: 2671

For: TEXTURE CACHE FOR A COMPUTER GRAPHICS ACCELERATOR

Commissioner for Patents
Washington, D.C. 20231

DECLARATION UNDER 37 CFR 1.131 BY CURTIS PRIEM, GOPAL SOLANKI, AND DAVID KIRK IN SUPPORT OF ANTEDATING REFERENCE

1. We are the inventors of the invention claimed in U.S. Patent Application No. 09/056,656, entitled "Texture Cache for a Computer Graphics Accelerator," filed April 7, 1998 ("the '656 application").

2. The '656 application discloses a graphics accelerator for use with a central processing unit (CPU) and a system bus, wherein the graphics accelerator includes a texture cache system.

3. The disclosed graphics accelerator was developed as part of NVIDIA's NV3 project.

4. The NV3 project produced the RIVA 128 product, which was publicly introduced on April 8, 1997 (see Exhibit A).

5. The RIVA 128 product was shipped to customers prior to March 26, 1998 ("the Critical Date").

6. NVIDIA's NV3 Graphics Reference Manual ("the Graphics Manual"), which was available prior to the Critical Date, described the interface to read and write the context of the graphics engine in the RIVA 128 product. Excerpts from the Graphics Manual are attached as Exhibit B.

7. The RIVA 128 product included a texture cache memory that stores texel data to be used by a graphic engine to produce texture values for pixels. This is reflected at pages 54-55 of the Graphics Manual, which refers to the CACHE_INDEX register that facilitates the writing and reading of the RAMs used in the graphic engine's texture cache, and to the CACHE_RAM register that facilitates as the data access port for the writing and reading of the RAMs used in the graphic engine's texture cache.

8. The RIVA 128 product included a cache controller that performs a replacement policy determination for texel data to be stored in a texture cache memory. This is reflected at pages 11-12 of the Graphics Manual, which refers to the CACHE_STATE bit that will reset the texture cache state machines in the graphics engine.

9. The RIVA 128 product included a DMA engine that retrieves texel data from memory. This is reflected at pages 40-41 of the Graphics Manual, which refers to the PORT_DMA bit, the DMA_ENGINE bit, and the DMA_NOTIFY bit within the status register. This is also reflected

at page 102 of the Graphics Manual, which refers to the DMA control registers such as the access register and the control register.

10. The texture cache memory of the RIVA 128 product was fully-associative.

11. The DMA engine of the RIVA 128 product implemented virtual-physical address translation. This is reflected at pages 103-104 of the Graphics Manual, which refers to the TLB_PTE register that includes the virtual to physical address translation lookaside buffer's page table entry, and to the TLB_TAG register that includes the virtual to physical address translation lookaside buffer's tag for the page table entry. This is also reflected at page 107 of the Graphics Manual, which refers to the DMA_START[] value that is used to create the offset value used by the DMA engine to calculate the virtual address of the intended access.

12. The RIVA 128 product included support for a prefetch mode and a non-prefetch mode. This is reflected at pages 15-16 of the Graphics Manual, which refers to the PREFETCH bit that enables or disables texture prefetching.

13. Prior to the Critical Date, the RIVA 128 product was included in a graphics accelerator board that operated in a system including a CPU, memory, and a system bus.

14. Prior to the Critical Date, the RIVA 128 product was used in a texture mapping method that retrieved texel data from memory via a direct memory access engine, stored retrieved texel

data in a texture cache memory based on a replacement policy determination performed by a cache controller, and rendered a polygon using texel data stored in the texture cache memory.

15. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Executed on: 5-16-02

Curtis Priem

Executed on: 5-16-02

Gopal Solanki

Executed on: 5/16/02

David Kirk